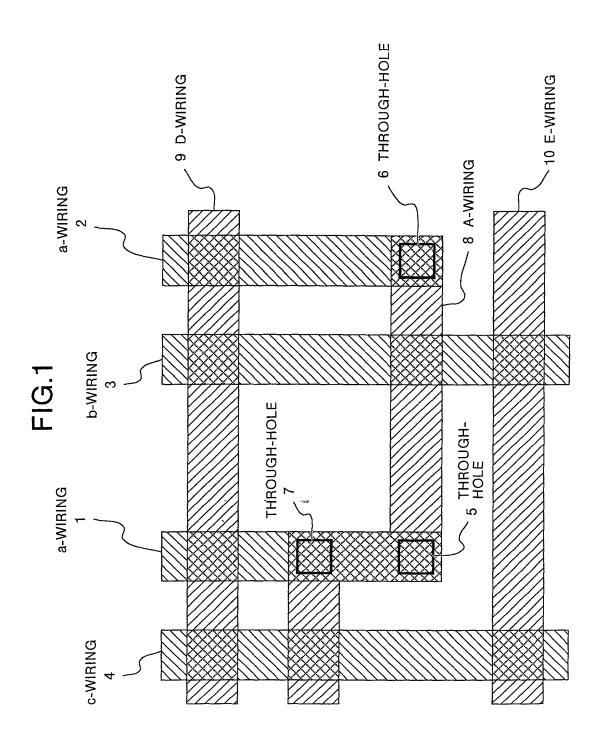
Title: METHOD OF WIRING SEMICONDUCTOR INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT, AND COMPUTER PRODUCT Inventors: Takao HASEGAWA Atty Docket No.: 401558

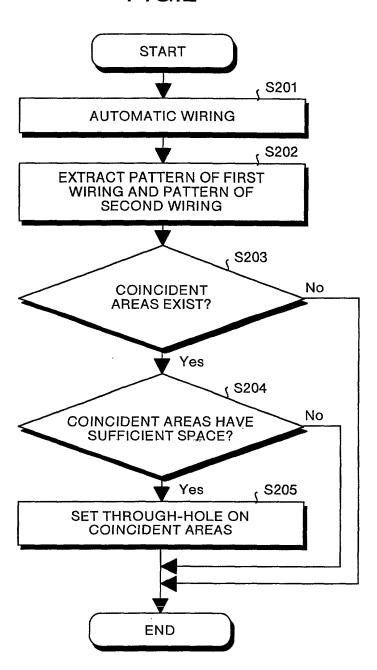
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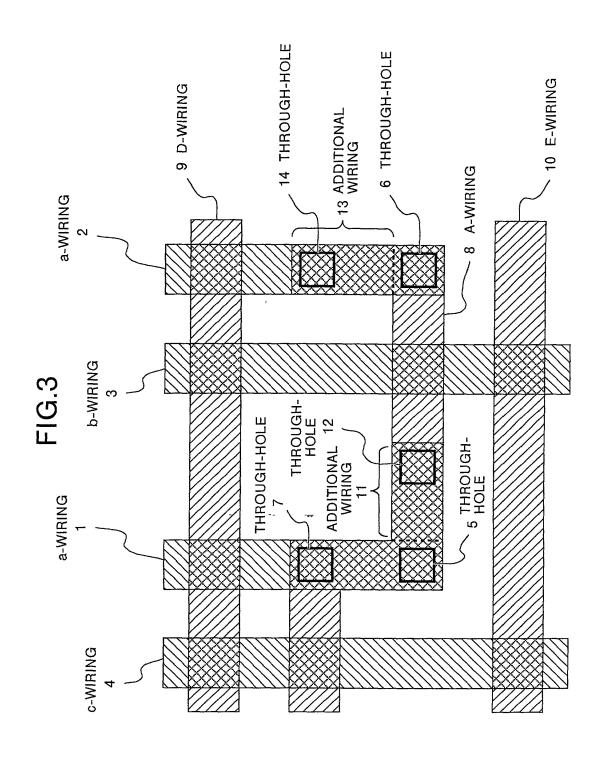
FIG.2



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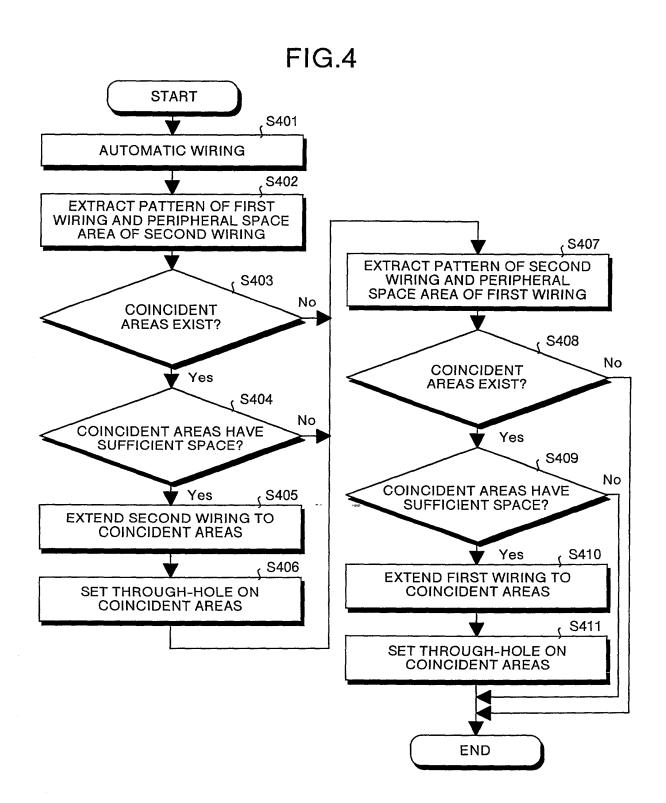


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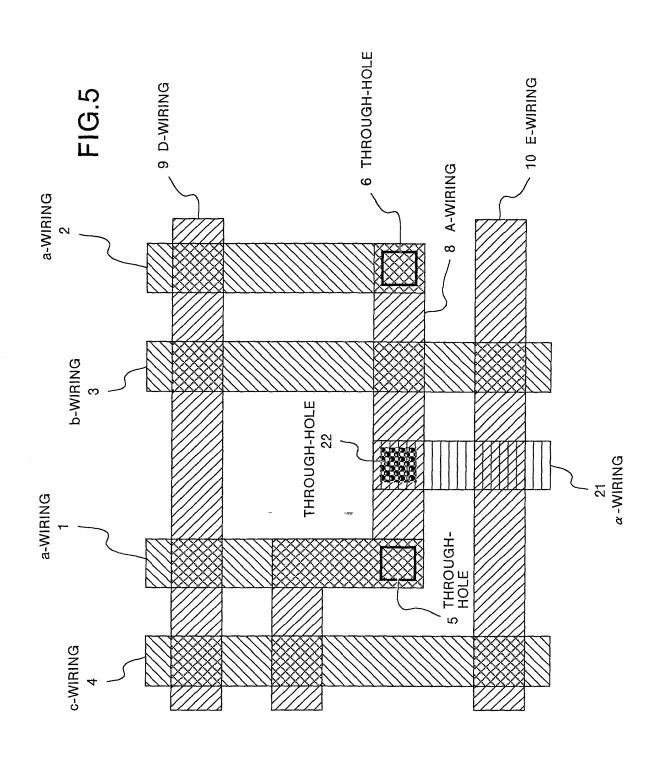
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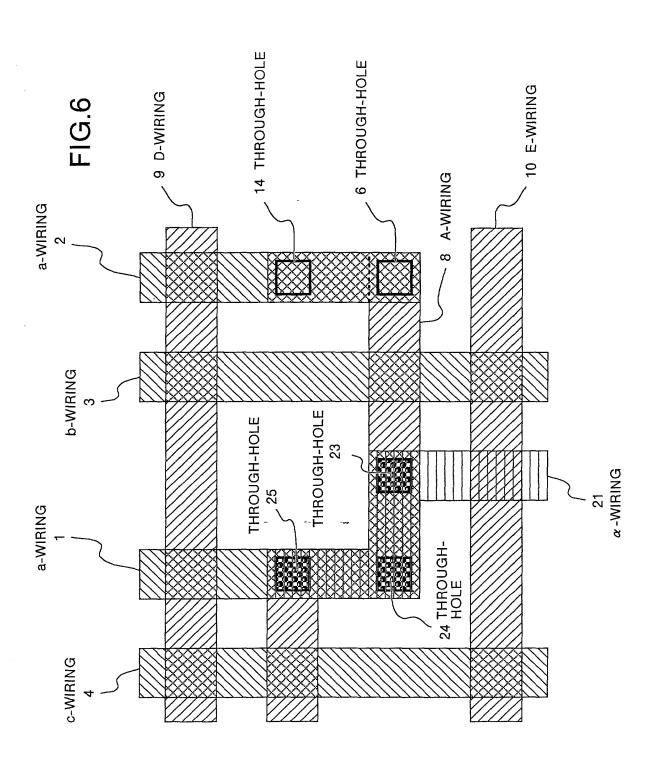
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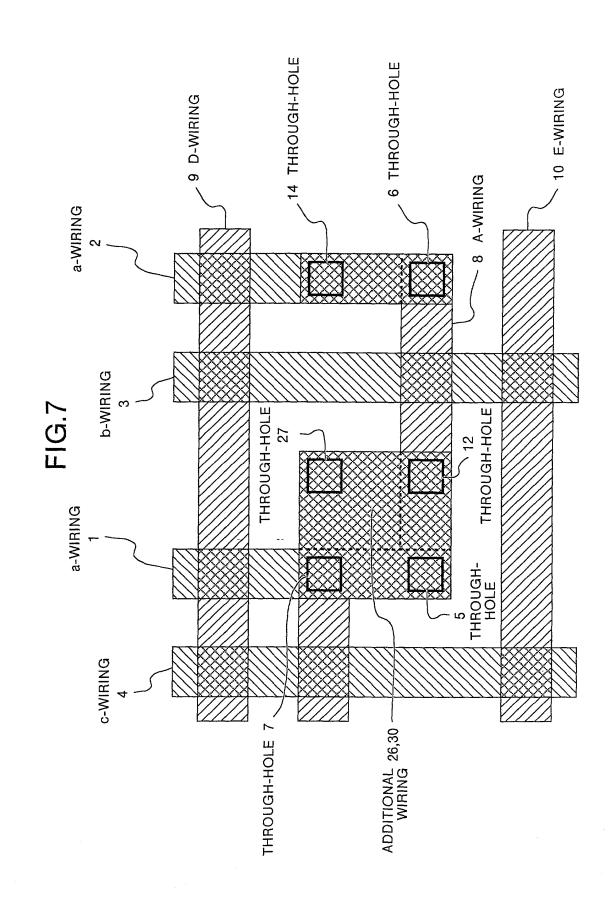
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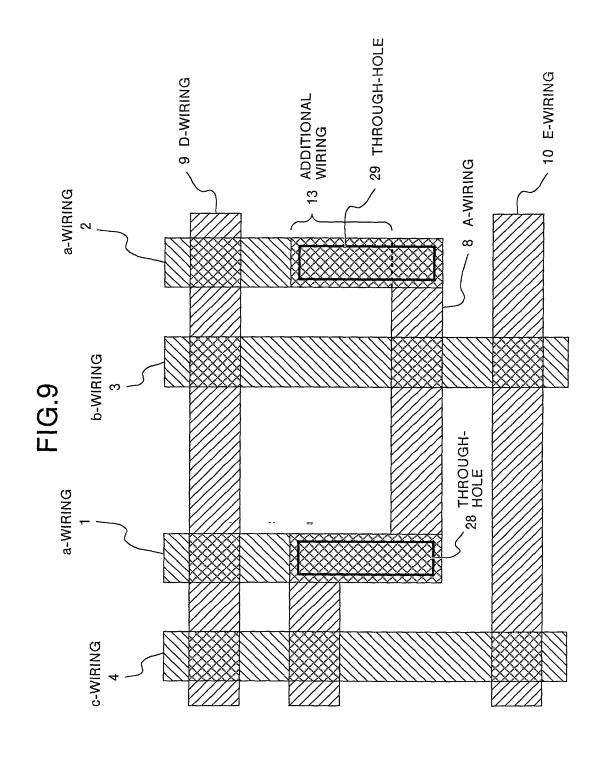
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FIG.8 **START** , S801 **AUTOMATIC WIRING** S802 EXTRACT PERIPHERAL SPACE AREA OF FIRST WIRING AND PERIPHERAL SPACE AREA OF SECOND WIRING S803 No COINCIDENT AREAS EXIST? Yes S804 No COINCIDENT AREAS HAVE SUFFICIENT SPACE? --S805 Yes EXTEND FIRST WIRING AND SECOND WIRING TO COINCIDENT AREAS S806 SET THROUGH-HOLE ON COINCIDENT AREAS **END**

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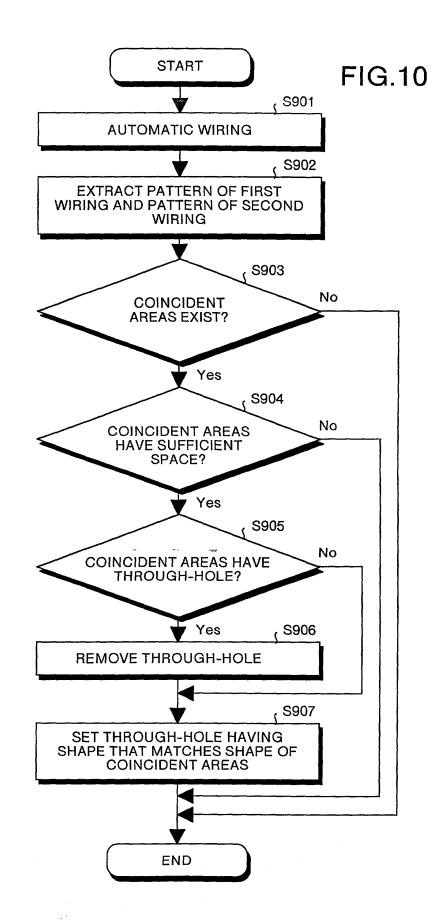


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